REMARKS

This paper is responsive to the Final Office Action dated July 12, 2004 in the above identified application for United States Patent. All rejections and objections of the Examiner are respectfully traversed. Reconsideration is respectfully requested.

At paragraphs 2 and 3 of the Office Action, the Examiner rejected claims 1-3, 5-6, 9-16 and 18 for obviousness under 35 U.S.C. 103, citing United States patent number 6,157,955 of Narad et al. ("Narad et al.") and United States patent number 6,157,996 of Christie et al. ("Christie et al."). Applicants respectfully traverse this rejection.

Narad et al. describe a system including rings of pointers for passing control of buffers indicated by the pointers, a status word including bit field definitions for indicating the status of a packet stored in memory buffers, a data structure that also may be used to store information about stored packets, and a programming model for providing access to stored packet data as a service. As noted in Applicant's response to the previous Office Action in the application, Narad et al. describe definitions of bit fields *in a status word reflecting the status of a packet in memory buffers*. Accordingly, the Examiner acknowledges in the current Office Action that Narad et al. includes no teaching or suggestion of indications of bit fields in source and target operands, or of manipulation of bits in any field of the source and target operands.

Christie et al. disclose a microprocessor for executing computer instructions including facilities for increasing the addressable register space, conditionally executing instructions based upon predicate information contained in the computer instruction, and operating in a three register operand mode in which the instruction operands include a first and second source

operand as well as a third destination operand. The teachings of Christie et al. include an embodiment in which the first and second source operands and the destination operand of the computer instruction are each indicated by 5-bit fields within the computer instruction. Three bits of the 5-bit destination operand of the Christie et al. system are contained within the lowest three bits of a prefix byte of the computer instruction, and the remaining two bits of the 5-bit field are contained within the highest two bits of a byte following an opcode byte of the computer instruction. Three bits of the 5 bit first and second operands described by Christie et al. are each contained within a byte following an opcode byte of the computer instruction and the remaining two bits of the 5 bit first and second operands are contained within a subsequent byte of the computer instruction.

Nowhere in the combination of Narad et al. and Christie et al. is there disclosed or suggested any system or method for direct access to bit fields in instruction operands, including:

> providing ***indications of bit fields in source and target operands of a processor executable instruction, each of the indicated bit fields consisting of a plurality of bits in a plurality of bit positions in the source and target operands***;
> performing the processor executable instruction utilizing the bit fields in the source and target operands in response to the indications of the bit fields ; and
> providing, by performing the processor executable instruction, and in response to the indications of the bit fields, ***direct manipulation of any bits in any bit field of the source and target operands***. (emphasis added)

As in the current independent claim 1. Independent claim 5 includes analogous features. In contrast, and as noted in the previously submitted response, the use in Narad et al. of bit definitions in a status word or control register is far different from the indications of bit fields in source and target operands of a processor executable instruction, as set forth in the present independent claims 1 and 5. Moreover, the system of Narad et al. uses a mask-and-rotate unit to

pre-process data to be used in operands in computations, as opposed to the present independent claims 1 and 5, in which ***indications of bit fields within source and target operands of a processor executable instruction are used to define bit fields at any location within the source and target operands themselves***. In further contrast to the present claims 1 and 5, Christie et al. describes a system in which operands are indicated by *bit fields of instructions*. As stated in column 17 of Christie et al., beginning at line 4:

> Accordingly, the embodiment of the three register operand extension described with respect to FIG. 12 details first and second source operands 1130 and 1132 respectively and a destination register field 1134 ***are each indicated by 5-bit fields within computer instruction 1101***. In one embodiment, three bits of the 5-bit destination operand 1134 are contained ***within the lowest three bits of a prefix byte of computer instruction 1101***. (emphasis added)

Thus Christie et al. is concerned with providing indications of operands, and a destination register, *by bit fields*, as opposed to the *indications of bit fields within operands for direct manipulation*, as in the present independent claims 1 and 5.

For the above reasons Applicants respectfully urge that the combination of Narad et al. and Christie et al. does not disclose or suggest all the features of the present independent claims 1 and 5. Accordingly, Narad et al. and Christie et al. do not support a *prima facie* case of obviousness under 35 U.S.C. 103 with regard to claims 1 and 5. As to dependent claims 2-3, 6, 9-16 and 18, they each depend from either claim 1 or claim 5, and are respectfully believed to be patentable over the combination of Narad et al. and Christie et al. for at least the same reasons.

At paragraph 4 of the Office Action, the Examiner rejected claim 4 for obviousness under 35 U.S.C. 103, again citing Narad et al., and also citing U.S. Publication No. 2003/0035430 A1 of Islam et al. ("Islam et al."). Applicants respectfully traverse this rejection.

Islam et al. describe a programmable network device that executes software modules resident on its hardware to support assorted applications and network management services. These modules of Islam et al. may be dynamically loaded, unloaded, or modified without interrupting network traffic routed through the device. The loading and unloading of modules in the Islam et al. system can be administered remotely, via a network backbone, service provider network, LAN, or other internetwork coupled to the device, or, alternatively, administrators may alter the operating parameters of individual management modules via the network to effect performance gains or modify existing operating parameters. The relevant teachings of Narad et al. are discussed above.

Nowhere in the combination of Narad et al. and Islam et al. is there disclosed or suggested any system or method for direct access to bit fields in instruction operands, including:

> providing ***indications of bit fields in source and target operands of a processor executable instruction, each of the indicated bit fields consisting of a plurality of bits in a plurality of bit positions in the source and target operands***;
>
> performing the processor executable instruction utilizing the bit fields in the source and target operands in response to the indications of the bit fields ; and
>
> providing, by performing the processor executable instruction, and in response to the indications of the bit fields, ***direct manipulation of any bits in any bit field of the source and target operands***. (emphasis added)

As in the present independent claim 5, from which claim 9 depends. Islam et al. contains no teachings regarding bit fields of any kind, and accordingly adds nothing further to the teachings of Narad et al. with regard to the above highlighted features of the presently claimed invention.

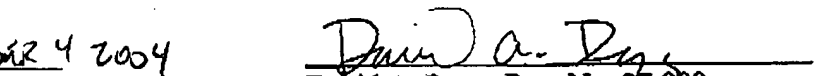
For the above reasons Applicants respectfully urge that the combination of Narad et al. and Islam et al. does not disclose or suggest all the features of the present independent claim 5, from which claim 9 depends. Accordingly, Narad et al. and Islam et al. do not support a *prima facie* case of obviousness under 35 U.S.C. 103 with regard to claim 5, and dependent claim 9 is respectfully believed to be patentable over the combination of Narad et al. and Islam et al. for at least the same reasons. Reconsideration of all pending claims is respectfully requested.

For these reasons, and in view of the above amendments, the Examiner's rejections are respectfully believed to be overcome, and it is respectfully requested that the rejections of the Examiner be withdrawn. This application is now considered to be in condition for allowance and such action is earnestly solicited.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone David A. Dagg, Applicants' Attorney at 978-264-6664 so that such issues may be resolved as expeditiously as possible.

Respectfully Submitted,

November 4 2004
Date



David A. Dagg, Reg. No. 37,809
Attorney/Agent for Applicant(s)
Steubing McGuinness & Manaras LLP
125 Nagog Park Drive
Acton, MA 01720
(978) 264-6664

Docket No. P269864 120-102
Dd: 09/12/2004